CLAIMS

What is claimed is:

1. A system for controlling peripheral devices in a computer system, the system for controlling peripheral devices comprising:

a microcontroller that provides a plurality of device interfaces, each of the device interfaces being adapted to support a peripheral device, and a communication interface that is adapted to allow communication between the communication interface and the peripheral devices; and

a device that stores programming instructions to initialize the microcontroller separately from the initialization of the computer system.

2. The system set forth in claim 1, comprising an auxiliary power source that supplies power to the microcontroller separately from a main power supply that supplies power to the system.

3. The system set forth in claim 1, wherein the communication interface comprises a Peripheral Component Interface ("PCI") interface.

4. The system set forth in claim 1, wherein the communication interface comprises an Extended Peripheral Component Interface ("PCI-X") interface.

5. The system set forth in claim 1, wherein the microcontroller comprises a Streamlined Advanced Programmable Interrupt Controller ("SAPIC") interface.

6. The system set forth in claim 1, wherein the microcontroller is adapted to provide power management functionality for at least one of the peripheral devices.

7. The system set forth in claim 1, wherein at least one of the peripheral devices is a Super I/O controller.

8. The system set forth in claim 1, wherein the microcontroller is defined to be a subtractive decode agent for the computer system.

9. The system set forth in claim 1, comprising reset logic that resets the system under control of the microcontroller.

10. The system set forth in claim 1, wherein the microcontroller provides emulation for at least one of the peripheral devices.

11. The system set forth in claim 1, comprising a local memory associated with the microcontroller.

12. A computer system, comprising:

a main power supply that provides power to the computer system;

a processor complex;

a system memory;

a memory controller that is connected to the processor complex and the system memory to retrieve data from the system memory for the processor complex;

a microcontroller that is connected to the memory controller, the microcontroller providing a plurality of device interfaces, each of the device interfaces being adapted to support a peripheral device, and a communication interface that is adapted to allow communication with the peripheral devices via the plurality of device interfaces; and

a device that stores programming instructions to initialize the microcontroller separately from the initialization of the computer system.

13. The computer system set forth in claim 12, comprising an auxiliary power source to supply power to the microcontroller.

14. The computer system set forth in claim 12, wherein the communication interface comprises a Peripheral Component Interface ("PCI") interface.

15. The computer system set forth in claim 12, wherein the communication interface comprises an Extended Peripheral Component Interface ("PCI-X") interface.

16. The computer system set forth in claim 12, wherein the microcontroller comprises a Streamlined Advanced Programmable Interrupt Controller ("SAPIC") interface.

17. The computer system set forth in claim 12, wherein the microcontroller is adapted to provide power management functionality for at least one of the peripheral devices.

18. The computer system set forth in claim 12, wherein at least one of the peripheral devices is a Super I/O controller.

19. The computer system set forth in claim 12, wherein the microcontroller is defined to be a subtractive decode agent for the computer system.

20. The computer system set forth in claim 12, comprising reset logic that resets the system under control of the microcontroller.

21. The computer system set forth in claim 12, wherein the microcontroller provides emulation for at least one of the peripheral devices.

22. The computer system set forth in claim 12, comprising a local memory associated with the microcontroller.

23. A method of controlling peripheral devices in a computer system, the method comprising the acts of:

initializing a microcontroller that includes a plurality of device interfaces, each of the device interfaces being adapted to support a peripheral device, the microcontroller comprising a communication interface

that is adapted to allow communication between the communication interface and the peripheral devices; and

programming the microcontroller separately from the computer system.

24. The method set forth in claim 23, comprising the act of providing auxiliary power to the microcontroller.

25. The method set forth in claim 23, comprising the act of defining a Streamlined Advanced Programmable Interrupt Controller ("SAPIC") interface for the microcontroller.

26. The method set forth in claim 23, comprising the act of employing the microcontroller to provide power management functionality for at least one of the peripheral devices.

27. The method set forth in claim 23, comprising the act of employing the microcontroller to communicate with a Super I/O controller via at least one of the device interfaces.

28. The method set forth in claim 23, comprising the act of defining the microcontroller to be a subtractive decode agent for the computer system.

29. The method set forth in claim 23, comprising resetting the system under control of the microcontroller.

30. The method set forth in claim 23, comprising emulating at least one of the peripheral devices.

31. A system for controlling peripheral devices in a computer system, the system for controlling peripheral devices comprising:

means for interfacing with a plurality of peripheral devices via a communication interface; and

a device that stores programming instructions to initialize the means for interfacing separately from the initialization of the computer system.

32. The system set forth in claim 31, comprising an auxiliary power source that supplies power to the means for interfacing.

33. The system set forth in claim 31, wherein the communication interface comprises a Peripheral Component Interface ("PCI") interface.

34. The system set forth in claim 31, wherein the communication interface comprises an Extended Peripheral Component Interface ("PCI-X") interface.

35. The system set forth in claim 31, wherein the means for interfacing comprises a Streamlined Advanced Programmable Interrupt Controller ("SAPIC") interface.

36. The system set forth in claim 31, wherein the means for interfacing provides power management functionality for at least one of the peripheral devices.

37. The system set forth in claim 31, wherein at least one of the peripheral devices is a Super I/O controller.

38. The system set forth in claim 31, wherein the means for interfacing is defined to be a subtractive decode agent for the computer system.

39. The system set forth in claim 31, comprising reset logic that resets the system under control of the means for interfacing with a plurality of peripheral devices.

40. The system set forth in claim 31, wherein the means for interfacing with a plurality of peripheral devices provides emulation for at least one of the peripheral devices.

41. The system set forth in claim 31, comprising a local memory associated with the means for interfacing with a plurality of peripheral devices.

42. A computer system that comprises a microcontroller that functions as a south bridge, the microcontroller being programmed to avoid conflicts with other devices and to reduce resource consumption.